**IN THE CLAIMS:**

Claims 1-22 (Canceled)

23. (Previously Presented) A process for fabricating an integrated circuit, comprising:

forming an oxide over a substrate, said oxide being defined by a width, said forming said oxide including

(a) exposing said substrate to a first oxidizing ambient, wherein exposing said substrate to a first oxidizing ambient includes increasing from an initial temperature to a first temperature below a threshold temperature at a first ramp rate, increasing from said first temperature to a second temperature below said threshold temperature at a second ramp rate, and growing at least a portion of said oxide;

(b) exposing said substrate to a second oxidizing ambient, wherein exposing said substrate to a second oxidizing ambient includes increasing from said second temperature to a third temperature at a third ramp rate, and increasing from said third temperature to a temperature above said threshold temperature at a fourth ramp rate; and

(c) cooling said substrate to a temperature below said threshold temperature, wherein said oxide and said substrate form an interface that is substantially stress free and planar;

forming within said substrate a source, a drain and a channel extending from said source to said drain, wherein said source and said drain do not include ~~a~~ lightly doped regions; and

forming a gate structure over said substrate, said gate structure having a length of approximately 1.25 μm or less and being coextensive with said width of said oxide.

24. (Previously Presented) A process as recited in claim 23, wherein said process further comprises forming said channel before forming said source and said drain.

Claim 25 (Canceled)

26. (Original) A process as recited in claim 24, wherein said channel is doped by a halo implantation.

27. (Original) A process as recited in claim 23, wherein said length is in the range of approximately 0.25 μm to approximately 0.05 μm.

28. (Previously Presented) A process as recited in claim 23, wherein said oxide layer has a first oxide portion and a second oxide portion.

29. (Original) A process as recited in claim 23, wherein a spacer is not formed adjacent said gate structure.

30. (Previously Presented) A process as recited in claim 23, wherein said oxide layer has a thickness in the range of approximately 1.5 nm to approximately 20.0 nm.

31. (Previously Presented) A process as recited in claim 23, wherein said source and said drain have doping levels in the range of approximately $1X10^{20}/cm^3$ to $5X10^{20}/cm^3$.

32. (Previously Presented) A process as recited in claim 23, wherein said channel has a doping level in the range of approximately $1X10^{16}/cm^3$ to approximately $1X10^{19}/cm^3$.

Claims 33-40 (Canceled)

41. (Previously Presented) The process as recited in claim 23, wherein said first temperature below said threshold temperature is approximately 750°C-850°C and said first ramp rate is approximately 50°C-125°C per minute.

42. (Previously Presented) The process as recited in claim 23, wherein said second temperature below said threshold temperature is approximately 800°C-900°C and said second ramp rate is approximately 10°C-25°C per minute.

43. (Previously Presented) The process as recited in claim 23, wherein said substrate is oxidizable silicon and said threshold temperature is the viscoelastic temperature of $SiO_2$.

44. (Previously Presented) The process as recited in claim 23, wherein step (b) further comprises:

increasing from said second temperature to said third temperature at a ramp rate of approximately 5-15°C per minute in an ambient oxygen concentration of approximately 0%-5%;

increasing from said third temperature to said temperature above said threshold temperature at a ramp rate of 5-10°C per minute in an ambient oxygen concentration of approximately 0%-5%; and

growing at least a portion of said oxide in an oxygen ambient concentration of about 25% or less.

45. (Previously Presented) The process as recited in claim 23, wherein step (c) further

comprises:

reducing from said temperature above said threshold temperature to approximately 800°C to 900°C at a rate of about 2°C-5°C per minute; and

reducing said temperature of approximately 800°C to 900°C to a boat pull temperature at a rate of about 35°C-65°C per minute, wherein said oxide portion formed in step (a) is a first oxide portion and acts as a stress sink to a second oxide portion formed in step (b) during at least a portion of said cooling.

46. (Previously Presented) The process as recited in claim 45, wherein said threshold temperature is the viscoelastic temperature of $SiO_2$.